What is claimed is:

1. A flip-chip package comprising:

a substrate having a top surface, a bottom surface and an opening passing through the top surface and the bottom surface;

a dummy die disposed on the bottom surface of the substrate corresponding to the opening, wherein the dummy die has a surface with a redistribution layer (RDL) electrically connected with the substrate and

a chip flip-chip mounted on the surface of the dummy die inside the opening, and electrically connected with the redistribution layer of the dummy die.

2. The flip-chip package of claim 1, further comprising a packaging body formed at the opening of the substrate.

3. The flip-chip package of claim 1, wherein the substrate is a printed circuit board.

4. The flip-chip package of claim 1, wherein the dummy die is larger than the chip in size.

5. The flip-chip package of claim 1, wherein the redistribution layer of the dummy die includes a plurality of flip-chip pads and a plurality of connecting pads arraying at the perimeters of the dummy die.

6. The flip-chip package of claim 5, wherein the flip-chip pads have a pitch smaller than that of the connecting pads.

7. The flip-chip package of claim 6, wherein the pitch of the flip-chip pads is smaller than 150 μm.

8. The flip-chip package of claim 5, further comprising a plurality of bonding wires connecting the connecting pads of the redistribution layer to the substrate.

9. The flip-chip package of claim 5, further comprising a plurality of bumps bonding the connecting pads of the redistribution layer to the substrate.

10. The flip-chip package of claim 1, further comprising a plurality of solder balls formed on the bottom surface of the substrate.

11. The flip-chip package of claim 10, wherein the substrate has a plurality of connection pads on the top surface electrically connected with the solder balls.

12. The flip-chip package of claim 11, further comprising a stack semiconductor package is disposed on the top surface of the substrate, the stack semiconductor package includes a plurality of outer terminals connecting with the connection pads.

13. The flip-chip package of claim 1, wherein the substrate has a stair around the opening.

14. The flip-chip package of claim 1, wherein the dummy die has an exposed surface corresponding to the surface with the redistribution layer, a thermal-conducting layer is formed on the exposed surface.

15. The flip-chip package of claim 14, wherein the thermal-conducting layer is a metal layer.

16. A chip carrier for flip-chip package comprising:

a substrate having an top surface, an bottom surface and an opening passing through the top surface and the bottom surface; and

a dummy die disposed on the bottom surface of the substrate corresponding to the opening, wherein the dummy die has a surface with a redistribution layer (RDL) electrically connected with the substrate.

17. The chip carrier for flip-chip package of claim 16, wherein the substrate is a printed circuit board.

18. The chip carrier for flip-chip package of claim 16, wherein the substrate has a stair around the opening.

19. The chip carrier for flip-chip package of claim 16, wherein the redistribution layer of the dummy die includes a plurality of flip-chip pads and a plurality of connecting pads, the connecting pads are arrayed at the perimeters of the dummy die.

20. The chip carrier for flip-chip package of claim 19, wherein the flip-chip pads have a pitch smaller than that of the connecting pads.

21. The chip carrier for flip-chip package of claim 19, wherein the pitch of the flip-chip pads is smaller than 150 μm.

22. The chip carrier for flip-chip package of claim 19, further comprising a plurality of bumps bonding the connecting pads of the redistribution layer to the substrate.

23. The chip carrier for flip-chip package of claim 16, wherein the dummy die has an exposed surface corresponding to the surface with the redistribution layer, a thermal-conducting layer is formed on the exposed surface.

24. The chip carrier for flip-chip package of claim 23, wherein the thermal-conducting layer is a metal layer.